

REMARKS

This Application has been carefully reviewed in light of the Final Office Action mailed November 28, 2006. At the time of the Final Office Action, Claims 1-21 were pending in this Application. Claims 1-21 stand rejected. Claims 1, 8, and 14 have been amended to further define various features of Applicants' invention. Applicants respectfully request reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102

Claims 1-21 stand rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication 2001/0050856 filed by Yasuro Matsuzaki ("Matsuzaki"). Applicants respectfully traverse and submit the cited art does not teach all of the elements of the claimed embodiment of the invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Furthermore, "the identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co. Ltd.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Applicant respectfully submits that the cited art as anticipated by the Examiner cannot anticipate the rejected Claims, because the cited art does not show all the elements of the present Claims.

Independent Claims 1, 8, and 14 have been amended to define that the first PLL unit provides an internal clock signal only to a first set of at least one of the circuit units and the second PLL unit provides an internal clock signal only to a second set of at least one of the circuit units. In other words, those circuit units obtaining the internal clock signal from the first PLL unit belong to the first set, while those circuit units obtaining the internal clock signal from the second PLL unit belong to the second set. Since the first set and the second set are mutually exclusive, it is clear that none of the circuit units belonging to the first set also may belong to the second set. Thus, none of the circuit units of the first set and the

second set obtains the internal clock signal from both the first PLL unit and the second PLL unit.

The Examiner stated that Matsuzaki discloses all the limitations of independent claims. Applicant respectfully disagrees. With respect to the memory module shown in Fig. 7 of Matsuzaki, all memory devices 120 to 127 obtain a clock signal from the first PLL unit 15 and from the second PLL unit 16. Accordingly, Matsuzaki does not teach a second set and a first set, which are mutually exclusive, as defined in the independent claims of the present application.

Because the amendments to the independent claims 1, 8 and 14 represent a mere clarification of the claim language, Applicant requests respectfully to enter the amendment.

CONCLUSION

Applicants have made an earnest effort to place this case in condition for allowance in light of the amendments and remarks set forth above. Applicants respectfully request reconsideration of the pending claims.

Applicants believe there are no fees due at this time, however, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-2148 of Baker Botts L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicant's attorney at 512.322.2545.

Respectfully submitted,
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Date: January 29, 2007

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